WHAT IS CLAIMED IS:

1. An interconnect for a semiconductor component comprising:

a substrate comprising a surface; and

a plurality of first contacts on the surface configured to electrically engage a plurality of second contacts on the component, and comprising electrically conductive silicon carbide layers.

2. The interconnect of claim 1 wherein the silicon carbide layers substantially cover the first contacts and areas of the substrate between adjacent first contacts.

3. The interconnect of claim 1 wherein the silicon carbide layers comprise a plurality of conductors configured for signal transmission.

4. The interconnect of claim 1 wherein the silicon carbide layers comprise doped silicon carbide.

5. The interconnect of claim 1 wherein the silicon carbide layers comprise oxidized silicon carbide.

6. The interconnect of claim 1 wherein the first contacts comprise projections configured to penetrate the second contacts.

7. The interconnect of claim 1 wherein the second contacts comprise bumps, and the first contacts comprise recesses configured to retain the bumps.

8. An interconnect for testing a semiconductor component comprising:

a substrate comprising a surface and a plurality of first contacts on the surface configured to electrically engage a plurality of second contacts on the component;

a plurality of electrically conductive silicon carbide conductive layers covering the first contacts and areas on the surface between adjacent first contacts;

a plurality of conductors on the surface in electrical communication with the silicon carbide conductive layer.

9. The interconnect of claim 8 wherein the silicon carbide layers comprise doped silicon carbide.

10. The interconnect of claim 8 wherein the conductors comprise oxidized silicon carbide.

11. The interconnect of claim 8 wherein the conductors comprise doped or oxidized silicon carbide.

12. The interconnect of claim 8 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors.

13. An interconnect for a semiconductor component comprising:

a substrate comprising a first surface and a second surface;

a plurality of first contacts on the first surface configured to electrically engage a plurality of second contacts on the component, the first contacts comprising projections covered with electrically conductive silicon carbide layers configured to penetrate the second contacts, the silicon carbide layers surrounding the projections and covering portions of the first surface proximate to the projections.

14. The interconnect of claim 13 wherein the silicon carbide layers comprise doped silicon carbide.

15. The interconnect of claim 13 wherein the silicon carbide layers comprise oxidized silicon carbide.

16. The interconnect of claim 13 wherein the silicon carbide layers comprise a plurality of conductors substantially covering the first surface.

17. The interconnect of claim 13 wherein the substrate comprises silicon and the projections comprise portions of the substrate.

18. The interconnect of claim 13 further comprising a plurality of electrically conductive vias in the substrate in electrical communication with the silicon carbide conductive layers.

19. An interconnect for a semiconductor component comprising:

a substrate comprising a first surface and a second surface;

a plurality of first contacts on the first surface configured to electrically engage a plurality of bumped contacts on the component, the first contacts comprising indentations covered with electrically conductive silicon carbide layers configured to retain the bumped contacts, the silicon carbide layers surrounding the indentations and covering portions of the first surface proximate to the indentations.

20. The interconnect of claim 19 wherein the silicon carbide layers comprise doped silicon carbide.

21. The interconnect of claim 19 wherein the silicon carbide layers comprise oxidized silicon carbide having an electrical resistivity of about 10^{-4} ohm-cm.

22. The interconnect of claim 19 wherein the silicon carbide layers comprise a plurality of conductors substantially covering the first surface.

23. The interconnect of claim 19 further comprising a plurality of electrically conductive vias in the substrate in electrical communication with the silicon carbide conductive layers.

24. A system for testing a semiconductor component comprising:

a testing apparatus comprising a base for retaining the component and a force applying mechanism attached to the base for applying a biasing force to the component; and

an interconnect on the base comprising a substrate having a surface, and a plurality of first contacts on the surface configured to electrically engage a plurality of second contacts on the component, the first contacts comprising electrically conductive silicon carbide layers surrounding the first contacts and covering portions of the surface.

25. The system of claim 24 wherein the silicon carbide layers comprise conductors configured for signal transmission and substantially covering the surface.

26. The system of claim 24 wherein the silicon carbide layers comprise doped or oxidized silicon carbide.

27. The system of claim 24 wherein the first contacts comprise projections configured to penetrate the second contacts.

28. The system of claim 24 wherein the first contacts comprise indentations configured to retain the second contacts.

29. A system for testing a semiconductor component comprising:

a testing apparatus comprising a wafer probe handler for applying a biasing force to the component and testing circuitry for applying test signals to the component;

an interconnect mounted to the wafer probe handler, the interconnect comprising a substrate and a plurality of first contacts on the surface configured to electrically engage a plurality of second contacts on the component, the first contacts comprising electrically conductive silicon carbide layers surrounding the first contacts and covering portions of the surface.

30. The system of claim 29 wherein the silicon carbide layers comprise doped or oxidized silicon carbide.

31. The system of claim 29 wherein the silicon carbide layers comprise conductors configured for signal transmission and substantially covering the surface.

32. A method for fabricating an interconnect for a semiconductor component comprising:

providing a substrate comprising a surface;

forming a plurality of first contacts on the surface configured to electrically engage a plurality of second contacts on the component;

at least partially covering the first contacts with electrically conductive layers comprising silicon carbide.

33. The method of claim 32 wherein partially covering the first contacts comprises deposition of doped silicon carbide using a chemical vapor deposition process.

34. The method of claim 32 wherein the conductive layers surround the first contacts and substantially cover areas on the substrate between adjacent first contacts.

35. The method of claim 32 further comprising forming a plurality of silicon carbide conductors on the surface in electrical communication with the conductive layers.

36. The method of claim 32 wherein the second contacts comprise planar pads and the first contacts comprise projections on the surface having penetrating projections for penetrating the second contacts.

37. The method of claim 32 wherein the second contacts comprise bumps and the first contacts comprise projections configured to penetrate the bumps.

38. The method of claim 32 wherein the second contacts comprise bumps and the first contacts comprise indentations configured to retain the bumps.

39. A method for fabricating an interconnect for a semiconductor component comprising:

providing a substrate;

forming a plurality of first contacts on the substrate configured to electrically engage a plurality of second contacts on the component;

forming electrically conductive silicon carbide layers on the first contacts, the silicon carbide layers substantially covering an area on the substrate between adjacent first contacts; and

forming a plurality of conductors on the substrate in electrical communication with the silicon carbide conductive layers.

40. The method of claim 39 wherein forming the silicon carbide layers comprises chemical vapor deposition of doped silicon carbide.

41. The method of claim 39 wherein forming the silicon carbide layers comprises oxidizing selected portions of a conformally deposited silicon carbide layer.

42. The method of claim 39 wherein the conductors comprise doped or oxidized silicon carbide.

43. The method of claim 39 further comprising forming a plurality of conductive vias in the substrate in electrical communication with the conductors.

44. The method of claim 39 wherein the first contacts comprise projections and the silicon carbide layers surround the projections and substantially cover areas on the substrate between adjacent projections.

45. The method of claim 39 wherein the component comprises an element selected from the group consisting of bare dice, chip scale packages, wafers containing

semiconductor dice, wafers containing chip scale packages, panels containing chip scale packages, boards containing semiconductor dice, and electronic assemblies containing semiconductor dice.

46. A method for fabricating an interconnect for a semiconductor component comprising:

providing a substrate comprising a surface;

forming a plurality of first contacts on the surface configured to electrically engage a plurality of second contacts on the component;

forming a mask on the surface comprising a plurality of openings aligned with the first contacts;

chemical vapor depositing doped silicon carbide layers through the openings onto the first contacts; and

removing the mask.

47. The method of claim 46 further comprising chemical vapor depositing doped silicon carbide conductors through the openings onto the surface for transmitting signals to the first contacts.

48. The method of claim 46 wherein the silicon carbide layers surround the first contacts and substantially cover areas on the substrate between adjacent first contacts.

49. The method of claim 46 wherein the substrate comprises a material selected from the group consisting of silicon, ceramic, plastic, silicon-on-glass, silicon-on-sapphire, gallium arsenide and germanium.

50. The method of claim 46 wherein the substrate and the first contacts comprise silicon projections configured to penetrate the second contacts.

51. The method of claim 46 wherein the second contacts comprise bumps, and the first contacts comprise silicon projections configured to penetrate the bumps.

52. The method of claim 46 wherein the second contacts comprise bumps and the first contacts comprise recesses in the substrate configured to retain the bumps.

53. The method of claim 46 wherein the component comprises an element selected from the group consisting of bare dice, chip scale packages, wafers containing semiconductor dice, wafers containing chip scale packages, panels containing chip scale packages, boards containing semiconductor dice, and electronic assemblies containing semiconductor dice.

54. A method for fabricating an interconnect for testing a semiconductor component comprising:

providing a substrate comprising a surface;

forming a plurality of first contacts on the surface configured to electrically engage a plurality of second contacts on the component;

conformally depositing a silicon carbide layer on the surface and on the first contacts;

forming a mask on the silicon carbide layer comprising a plurality of openings;

etching the silicon carbide layer through the openings to define a plurality of silicon carbide layers on the first contacts; and

oxidizing the silicon carbide layers to increase an electrical resistivity thereof.

55. The method of claim 54 wherein the oxidizing step is performed by thermal heating of the silicon carbide layers using a focused laser beam.

56. The method of claim 54 wherein the etching step defines silicon carbide conductors for transmitting signals to the first contacts.

57. The method of claim 54 wherein the etching step defines silicon carbide conductors for transmitting signals to the first contacts, the conductors substantially covering the surface of the substrate.

58. The method of claim 54 wherein the first contacts comprise silicon projections and the silicon carbide layers surround the projections and areas on the substrate between adjacent projections.

59. The method of claim 54 wherein the first contacts comprise indentations in the substrate and the silicon carbide layers surround the indentations and areas on the substrate between adjacent indentations.

60. The method of claim 54 wherein the substrate comprises silicon and further comprising forming an insulating layer on the substrate and the first contacts prior to the conformally depositing step.

61. A method for fabricating an interconnect for a semiconductor component comprising:

providing a substrate comprising a first surface and an opposing second surface;

forming a plurality of first contacts on the first surface configured to electrically engage a plurality of second contacts on the component;

forming silicon carbide conductive layers on the first surface, the conductive layers surrounding the first contacts and areas of the substrate between adjacent first contacts;

directing a laser beam at the silicon carbide conductive layers to increase their electrical conductivity;

forming a plurality of conductive vias in the substrate in electrical communication with the silicon carbide conductive layers; and

forming a plurality of terminal contacts on the second surface in electrical communication with the conductive vias.

62. The method of claim 61 wherein the silicon carbide layers substantially cover the first surface.

63. The method of claim 61 wherein the substrate and the first contacts comprise silicon.

64. The method of claim 61 wherein forming the silicon carbide conductive layers comprises chemical vapor deposition through a mask.

65. The method of claim 61 wherein forming the silicon carbide conductive layers comprises etching of a layer of silicon carbide conformally deposited on the surface.